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PATENT
P56077
01/21/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KWANG-JIN YANG *et al.*

Serial No.: 09/621,009

Examiner: *to be assigned*

Filed: 20 July 2000

Art Unit: 2733

For: BIT-RATE INDEPENDENT OPTICAL RECEIVER AND METHOD THEREOF

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JAN 21 2003

Technology Center 2600

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

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TC 2800 MAIL ROOM

Pursuant to 37 C.F.R. §§ 1.56, and 1.97 and 1.98 applicant cites, lists, and discusses and encloses copies of the following art references cited in an Examination Report from the Japanese Patent Office issued on the 12th of November 2002 in corresponding Japanese patent application No. 2000-183451.

JAPANESE PATENT REFERENCES:

<u>Publication No.</u>	<u>Inventor</u>	<u>Published Date</u>
• JP 09-018461	Oike <i>et al.</i>	17 January 1997
and English language Abstract for JP 09-018461		
• JP 10-224335	Kawano	21 August 1998

and English language Abstract for JP 10-224335

OTHER DOCUMENTS:

- Office action and *Notification of the Reasons for Objection* issued by the Japanese Patent Office on the 14th day of November 2002 in applicant's corresponding co-pending Japanese patent application assigned serial No. 2000-183451.

DISCUSSION

Oike '461 which was cited by the *Notice of the Reasons for Objection*, contemplates a controller that the task edges of the signal during a prescribed period in a preamplifier and measures the time interval of the edges. The determination subsequently made of whether in transmission rate is a high rate or a low rate, and the transmission rate determination is applied to the decoder.


Kawano '335 which was also cited by the *Notice of the Reasons for Objection*, discusses a bit phase detection circuit unaffected by the phase margin of a D-type flip-flop circuit, and uses a data change point detection circuit constructed with a delay circuit and unexclusive OR circuit generating a detection signal, and an AND circuit acquires an AND between the pulse of a clock signal. The phase detection signal remains a single state as long as the clock signal is separate from the data signal, and indication is generated when the data signal is close to the edge of clock signal.

Pursuant to 37 CFR § 1.97 (e)(1), each item of information contain the Information Disclosure Statement was first cited in any communication from a foreign patent office in a

counterpart foreign patent application not more than three months prior to the filing of the Information Disclosure Statement.

No fee is incurred by filing this Information Disclosure Statement.

Respectfully submitted,


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